PBK 203 02/1
Telecom switched mode power supply regulator

Description

PBK 203 02/1 is a monolithic control circuit intended for unisolated buck-mode (step-down) DC/DC-converters. It works directly of a high voltage power supply (-38V to -80V) making it ideal for use in telecom line-card applications. It includes all necessary functions to achieve a high performance solution with a minimum of external components. PBK 203 02/1 includes a N-channel power-DMOSFET switch.

Key Features

- Current mode control with internal slope compensation
- External programmed softstart/ softstopp
- Internal power-DMOS as switch
- Over temperature protection (OTP)
- Under voltage lockout (UVL)
- Alarm output for OTP and current limit

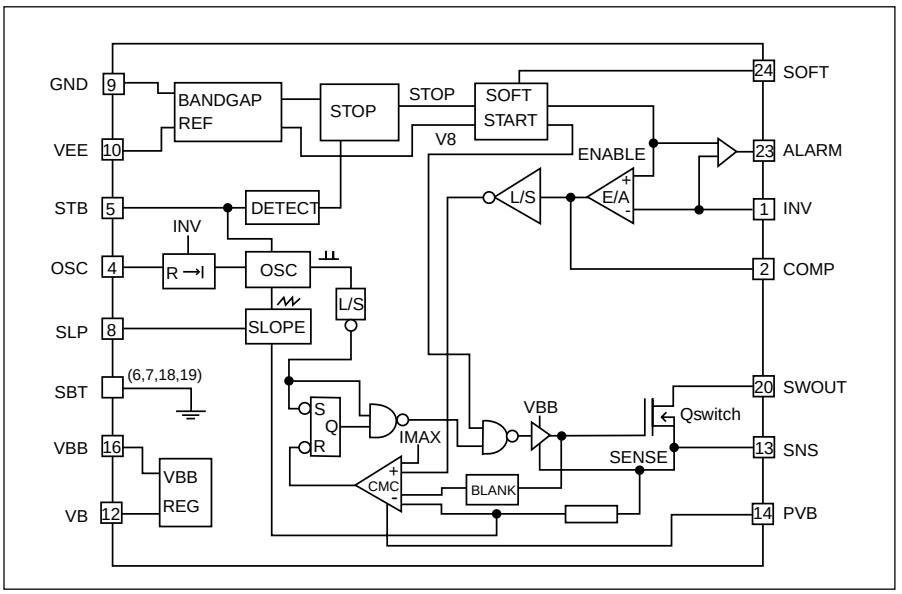
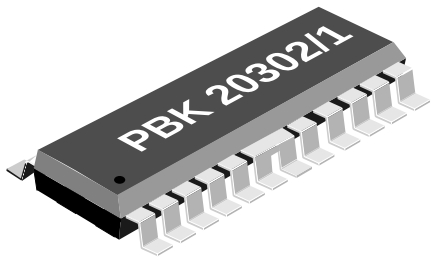


Figure 1. Block diagram.



24-pin batwing SOIC package

Maximum Ratings

Parameter	Pin No.*	Symbol	Min	Max	Unit
Voltage					
Input supply voltage	12	VB	-80		V
Digital inputs voltage	5	VS	0	6.5	V
Digital output pull-up voltage	23	VA	0	6.5	V
Digital output sink current		I_A	300		uA
Error amplifier input			-9	0	V
Error amplifier max output current			-1	1	mA
Output driver currents					
peak				2	A
continuos				0.7	A
Storage temperature			-55	+150	°C
Junction temperature			-35	+150	°C

Recommended Operating Conditions

Parameter	Pin No.*	Symbol	Min	Max	Unit
Ambient temperature range			0	+70	°C
Oscillator frequency			100	600	kHz
Frequency programming resistor		RT	70	300	kΩ
Current sense resistor			0.39		Ω

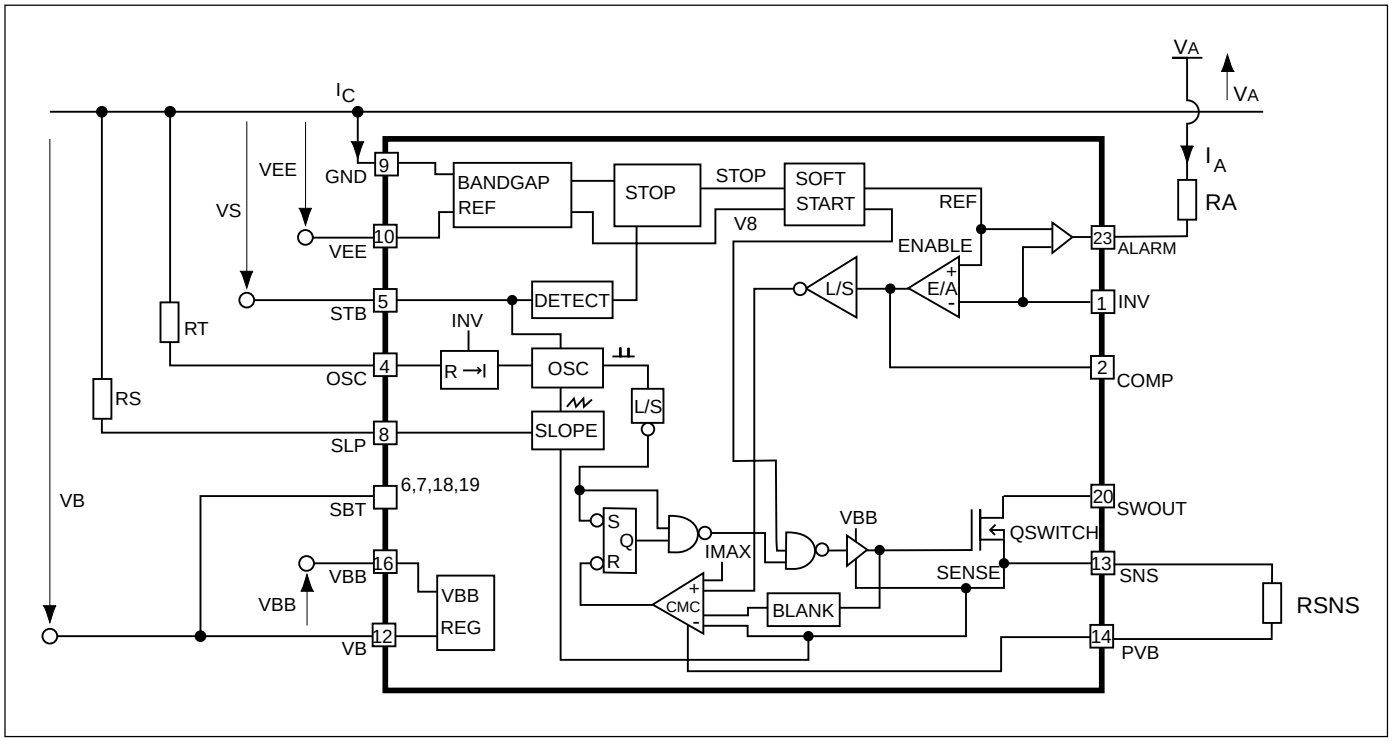


Figure 2. Definition of symbols

Electrical Characteristics

Electrical characterstics over recommended operating conditions, unless otherwise noted -0°C, CT: ≤ 70°C, ambient

Parameter	Pin No.*	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage (VB)	12	VB		-80		-38	V
Supply Current							
Ic		I_C			3.5	6	mA
Ic-standbye, Note 1					1.5		mA
Voltage Reference							
VEE T=25°C	10	VEE		-11.10	-10.90	-10.65	V
VEE				-11.10	-10.90	-10.65	V
VBB	16	VBB		8	10	12	V*
VEE- Short circuit current				1.5		10	mA
VBB-short circuit current				3		10	mA
* measured with respect to VB							
Under voltage lockout							
Stop Threshold				-35		-31	V
Hysteresis				2.5		4.7	V
Over temperature protection							
Stop Threshold				130		150	°C
Hysteresis				10		30	°C
Softstart							
Power-on-delay				0.2	0.6	2	ms
Start/ Stopp -time			CSOFT=2.2 nF		3.0		ms
Standby delay at 500 kHz				5		7	µs
Oscillator section							
Initial frequency, Fi			RT=90kΩ	425	475	525	kHz
Temperature stability			RT=90kΩ	-3		+3	%
STB logic ‘0’				0		1	V
STB logic ‘1’		VS		2.5		6.5	V
STB Pin impedance				20		40	kΩ
Slope compensation							
slope amplitude (p-p)			RS=18kΩ		320		mV
slope duty cycle				85		95	%

Notes

1. Not covered by final test programme.

Electrical Characteristics

Electrical characterstics over recommended operating conditions, unless otherwise noted -20°C, CT: ≤ 125°C

Parameter	Pin No.*	Symbol	Conditions	Min	Typ	Max	Unit
Comparator section							
Delay SNS to SWOUT				200		240	ns
Blanking time				40		100	ns
Error amplifier							
Open Loop Gain					85		dB
Bandwidth				800	1000	1300	kHz
Input common mode range					0	-9	V
Output range					-9.5	-8	V
Max output current					-1	1	mA
INV startpoint for frequency decrease	1	INV		-5.1		-4.9	V
Frequency decrease rate (% of Fi/INV)				20	25	30	%/V
Max frequency decrease (% of Fi)					25		%
Offset (including softstart error)				-25		+25	mV
Alarm							
Current limit alarm level (INV rel V8)				-4		-15	%
Sink current					0.5		mA
Logic low voltage (Ia=0.5mA)				0		1	V
Pull-up voltage		VA				6.5	V
Power DMOSFET							
Switch-fet RON			T=27°C	0.7	0.9	1.2	Ω
Switch-fet RON				0.5		2.0	Ω

Thermal Charactenstics

Parameter	Pin No.*	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance			24 SOIC BW		13		K/W
Power losses			24 SOIC BW		1.5		W

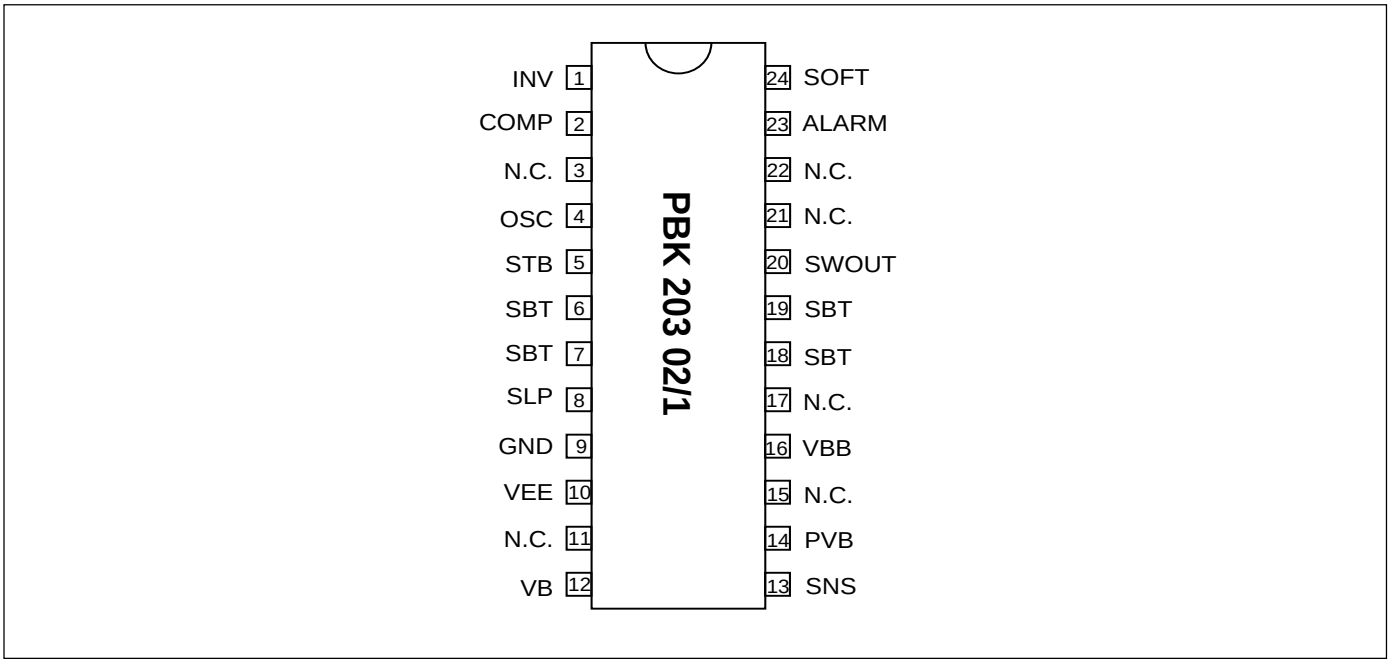


Figure 3. Pin configuration.

Pin description

SO	Symbol	Description
1	INV	Inverted input to error amplifier. The error amplifier has a bandwidth of typical 1MHz.The noninverted input is internally connected to a reference voltage. The reference voltage is at softstart decreased from 0V to -8V. The slope length TSOFT depens on the external capacitor CSOFT, TSOFT(ms) = 1.4·CSOFT(nF)
2	COMP	This is the output of the error amplifier as well as input to the current mode PMW-comparator. The level at COMP sets the peak output current from the switch . Connect a RC-link between COMP and INV to set the regulator loop compensation. The normal output range at COMP is -8V to -9V.
3	N.C.	
4	OSC	The oscillator uses an internal capacitance and an external resistor to set the regulator switching frequency. The external resistor is connected between RT and GND and sets the frequency according to the following equation: f(kHz)=44000/RT(kΩ). Recommended operating frequency is maximum 600kHz.
5	STB	The regulator is set to standby mode if STB is connected to a Logic high level (+3V to +6.5V, relative to GND).
6,7	SBT	SBT shall be connected to VB with either pin 6 and 7 or pin 18 and 19.
8	SLP	Slope compensation is needed to prevent instability when duty cycle is above 50%. Slope compensation is added to the sensed current signal. The amount of slope compensation is programmed with an external resistor between RS and GND. The slope length is 90% of the oscillator period. The slope peak to peak value is set according to the following equation: Uslope(V) = 9 / RS (KΩ).
9	GND	All voltages are measured with respect to GND.
10	VEE	The control circuit includes a linear regulator for internal power supply of the circuit. This voltage is accessible at VEE and should be bypassed to GND with a ceramic low ESL capacitor. VEE = -11V. VEE is generated with a bandgap reference and has an accuracy of +/- 3%. VEE can be externally loaded with maximum 1mA. The internal reference voltage to the error amplifier is derived directly from VEE (via softstart).
11	N.C.	
12	VB	The power supply - battery voltage - is connected to VB. VB should be bypassed to GND with a ceramic, low ESL capacitor. The maximum battery voltage is -80V. At voltages bellow -35V the under voltage lockout will disable the driver to the DMOSFET resulting in a high impedance output at SWOUT.
13	SNS	A current sense resistor should be connected between SNS and PVB. Maximum current is programmed with the value of the resistor. The internal current limit level is set to 0.5V measured at SNS with respect to PVB.

Pin description

SO	Symbol	Description
14	PVB	Power supply connection to power switch. PVB should be connected via an inductor to VB.
15	N.C.	
16	VBB	The power to the DMOSFET driver is supplied from VBB. VBB is approximately 10V above VB. VBB should be bypassed to VB with a ceramic, low ESL capacitor.
17	N.C.	
18,19	SBT	SBT shall be connected to VB with either pin 18 and 19 or 6 and 7.
20	SWOUT	Switching power output. Recommended output current is up to 700 mA.
21,22	N.C.	
23	ALARM	To use the alarm output a pull-up resistor should be connected from ALARM to a logic level power supply (3V to 6.5V). ALARM is forced low if the over temperature protection (OTP) is activated or if the regulator works in the current limit mode. The OTP is activated if chip temperature is above 130°C and it has an hysteresis of minimum 10 °C.
24	SOFT	An external softstart/softstopp capacitor shall be connected between SOFT and GND. The start/stopp time is set according to the following equation: TSOFT (ms) ≈ 1.4•CSOFT (nF). Softstopp is activated only with the STB signal. At softstopp the output voltage is decreased from nominal voltage to near zero voltage. At an output voltage <4% of nominal output voltage the output drive are disabled.

Functional description

PBK 20302 is a current mode regulator with fixed frequency. It has good load transient response and automatic feed-forward compensation.

Slope compensation, necessary for operation with duty cycle >50%, is provided by an internal slope compensation circuit that is programmed with an external resistor. Current mode control makes it possible to current limit the regulator pulse by pulse. A blanking circuit disables the current mode comparator for the leading edge of the current sense signal. This eliminates the need for an external current sense filter. Minimum on-time is limited by the blanking time and propagation delay from the current mode comparator to SWOUT and is approximately 200ns. The characteristics of the current limit is improved by a decrease in switching frequency when the regulator is short circuited.

The decrease in switching frequency starts when output voltage is 5/8 of nominal value. It decreases linear to nominal frequency divided by of 4 when output voltage reaches 15% of nominal output voltage. This prevents the output current to raise uncontrollable when the output is short circuit. Switching frequencies up to 600kHz is possible. Duty cycle on the switch DMOSFET is maximised to 90%.

The regulator includes an Over Temperature Protection (OTP) with hysteresis . An Under Voltage Lockout (UVL) shuts of the regulator when the input voltage is below 35V. The STB input can be used to set the regulator in standby mode. The OTP can be monitored at the ALARM output from the regulator. The ALARM output also indicate if the regulator works in current limit. When OTP, UVL or STB is true the driver to the switch and are disabled and softstart is reset. When OTP, UVL and STB turns false softstart is performed after a delay of approx. 1 ms. The softstart ramps the reference voltage to the error amplifier with a slope that depend on the external capacitor CSOFT. When the requlator is set to standby mode the reference voltage decrease with the same slope. The drivers to the switch is then disabled when the reference to the error amplifier is below -0.3V.

The error amplifier has high impedance inputs. The bandwith is typical 1 MHz. The output and INV input is accesible for loop compensation. The output is level-shifted /inverted to the current mode comparator.

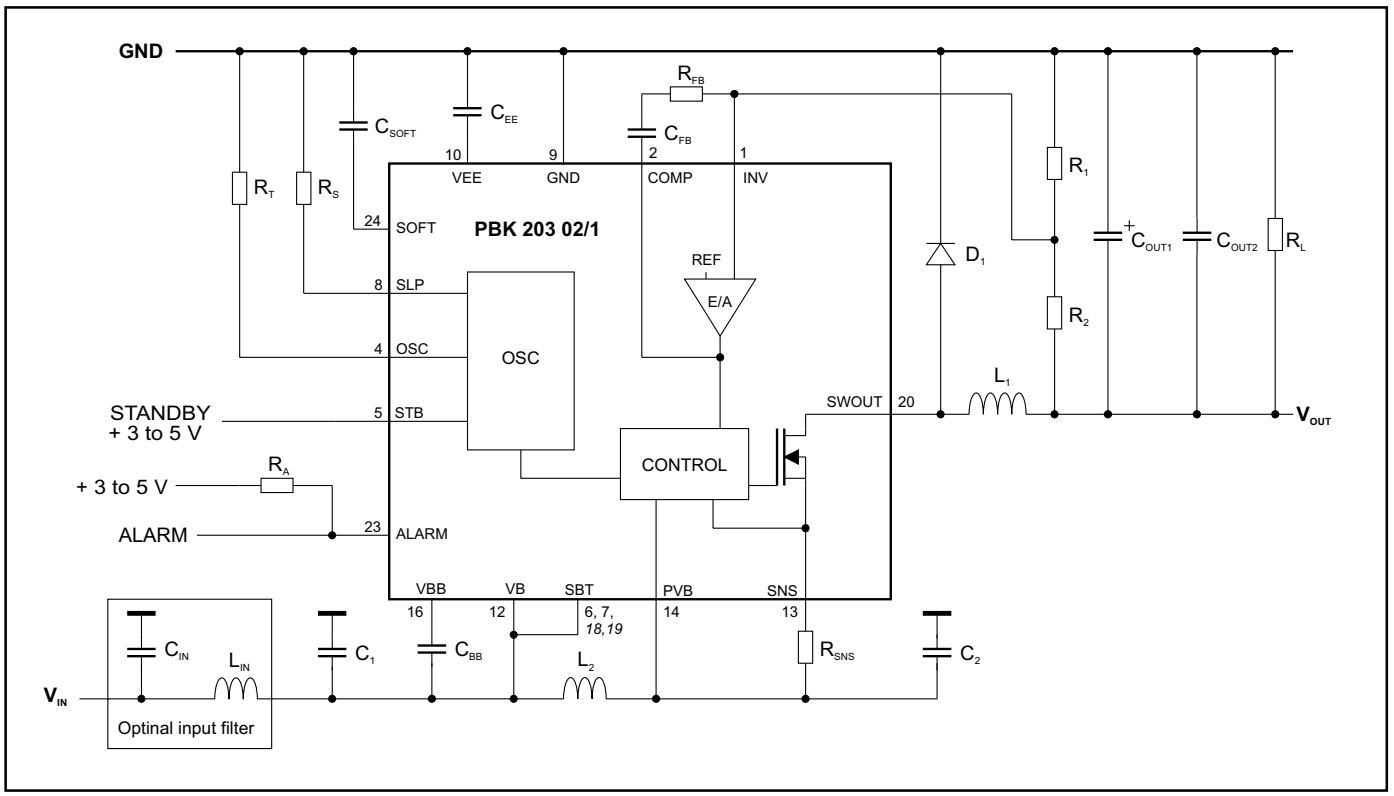


Figure 4. Typical step-down converter application.

Application Information

Description Of A Typical Step-down Converter Application

L_1 and the C_{OUT} capacitors are working as the output "filter". D_1 is the freewheeling diode.

R_1 and R_2 are feeding the output voltage back to the error amplifier and are used to program the output voltage. C_{FB} and R_{FB} are working together with R_1 and R_2 as network in the voltage feedback loop.

C_1, L_2 and C_2 are working as an input filter protecting the input voltage from noise. C_{IN} and L_{IN} could be used if extra protection is needed for the input voltage.

C_{EE} and C_{BB} are stabilising internal voltages in the circuit.
R_{SNS} is working as current feedback and is programming the maximum output current. R_T is setting the switching frequency.

R_S is used to set an internal slope compensation ramp to make the application stable when working with a duty cycle >50% (i.e. Vout/Vin>50%).
C_{SOFT} is used to set the soft start and soft stop time.

Pin 5, STB, which is the standby input, could be used to put the circuit in standby when connected to +3V or +5V. If standby isn't going to be used it's recommended that pin 5 is connected to GND.

Pin 23, alarm, should be connected with a 20kΩ pull up resistor to +3V or +5V if the alarm function is going to be used. Pin 23 will then be pulled low if the circuit is working in current limit mode or if the circuit temperature is higher than 130 °C.

Components You Usually Don't Have To Change

Internal voltages stabilised with C_{EE} and C_{BB}

C_{EE} and C_{BB} are used to stabilise internal voltages and should both be 100nF cer.

Input filter - C_1, L_1 and C_2 with optional C_{IN} and L_{IN}

C_1, L_2, and C_2 are used as an input filter protecting the input voltage from noise from the switch. With C_1 = 470 nF cer, L_2 = 10 µH, C_2 = 680 nF cer the ripple on the input voltage will be ~ 80 mV_{P-P}. By using an extra input filter with C_{IN} = 330 nF cer and L_{IN} = 10 µH the input ripple will be reduced to ~30 mV_{P-P}. The above figures yield when using a switched power supply as input voltage. Other voltage sources might give other result depending on what kind of output impedance the voltage source has and what kind of impedance the distribution system have. C_{IN} or L_{IN} could of course be increased to get an even smaller disturbance on the input voltage.

C_2, which is connected to PVB, pin 14, is very important for the stability in this point, because PVB is used as a virtual ground for the current feedback.

Therefore should C_2 be connected close to the circuit and have short way to GND.

Setting the switching frequency with R_T

The resistor RT is setting the switching frequency by the formula:

$$R_T\ (k\Omega) = \frac{44000}{F(k\Omega)}$$

To be able to use the recommended output filter and error amplifier network as below the switching frequency should be ~ 450 to 500 kHz. This would give an $R_T \approx 90\ k\Omega$.

Output filter - L2, C_{Out1} and C_{Out2}

The output filter consists of L_2, C_{Out1} and C_{Out2}. The components values, L_2 = 68 µH, C_{Out1} = 47 µF elyt and C_{Out2} = 470 nF cer, has been calculated and verified for an output voltage of ~ -20 to -30V and with an input voltage range from ~ -38 to -80 V.

The error amplifier network - R_{FB} and C_{FB}.

RFB and CFB are designed considering the above switching frequency and output filter. The components values, R_{FB} = 30 kΩ and C_{FB} = 10 nF cer, has been calculated and verified for an output voltage of ~ -20 to -30V and with an input voltage range from ~ -38 to -80V.

Minimum output current - R_L

Since the DC/DC application could be seen as a current source with the switch inductor L_1 as the current sourcing component and that the circuits duty cycle (on time of the switch) not can be zero, there will be a minimum load current. Therefore the resistor R_L has been put between the output voltage and ground working as a dummy load of about 9-10mA.

Components that you use to program the application

If you use the standard values as described above and the application according to figure 4 there are just five component values to calculate, R_1, R_2, R_{SNS}, R_S, and C_{SOFT}.

Setting the output voltage with R_1 and R_2

R1 and R2 set the output voltage. Two equations are needed:

(1a) $V_{Out} = -8 \cdot \frac{R_1 + R_2}{R_1}$

Note ! V_{Out} is negative.

(1b) $R_2 = \frac{R_1 \cdot V_{Out}}{8} + R_1$

(2) $R_1 \,//\, R_2 \approx R_{FB} \cdot 2$; R_{FB} = 30 kΩ

In equation (1) the -8 is the internal reference voltage. By setting the resistor ladder R_1, R_2 to scale the output voltage to -8V the output voltage is programmed. R_1 and R_2 together with R_{FB} are forming the voltage feedback loop. Therefore you have to use the equation (2) to be able to get the right amplification in the loop. The easiest way to calculate the resistor values is to start with R1 = 100 kΩ and then check the parallel value of R_1 and R_2 which should be $\approx R_{FB} \cdot 2$. These calculations might have to been done a couple of times to get the right parallel value to match R_{FB}.

Setting max output current with R_{SNS}

Using the R_{SNS} = 0.39 Ω will give a maximum output voltage of 700 mA. Increasing the R_{SNS} to 0.82 Ω will give a maximum output current to about 350 mA. This yields with an nominal input voltage of -48V.

Setting the slope compensation with R_S

R_S is setting internal slope compensation and is affected by the output voltage and switch inductor L_1 that has been chosen for the application. It's recommended that R_S always is set even when the duty cycle is < 50 %, e.g. V_{OUT}/V_{IN} < 50 %.
The formula to use is:

$$R_S = \frac{1}{23} \cdot \frac{V_{Out}}{L_1}$$

Setting the soft start and soft stop time with C_{SOFT}

$T_{Soft}\ (ms) = 1.4 \cdot C_{Soft}\ (nF)$

A 2.2nF ceramic capacitor will give a soft start time of about 3ms.

Design examples

In the below design examples following data yields:

Input voltage range	-38 to -80V
Maximum output current	700mA
Soft start and soft stop	~3ms
Switching frequency	~450-500kHz.
Output voltage accuracy	< +/- 0.5V
Output impedance	< 10Ω
Output voltage ripple	< 90mV rms
Input voltage ripple	< 60mV rms
Input voltage ripple	< 20mV rms with optional input filter
PSRR	>40dB (0-20 kHz)

Component values that differ between the two examples are in bold font.

Example of a -48/-24 V step down application		
R_1 = 100 kΩ	0.2%	C_1 = 470 nF, cer
R_2 = 200 kΩ	0.2%	C_2 = 680 nF, cer
R_T = 90 kΩ		C_{OUT1} = 47 µF, elyt
R_S = 15 kΩ		C_{OUT2} = 470 nF, cer
R_{FB} = 30 kΩ		C_{SOFT} = 2.2 nF 50V, cer
R_A = 20 kΩ		C_{FB} = 10 nF 50V, cer
R_L = 2.7 kΩ		C_{BB} = 100 nF 50V, cer
R_{SNS} = 0.39 Ω		C_{EE} = 100nF 50V, cer
L_1 = 68 µH, 1A		
L_2 = 10 µH, 1A		
D_1 = 1A, 90V schottky		
Optional input filter:		C_{IN} = 330n, cer
		L_{IN} = 10µH, 1A
Example of a -48/-28 V step down application		
R_1 = 100 kΩ	0.2%	C_1 = 470 nF, cer
R_2 = 250 kΩ	0.2%	C_2 = 680 nF, cer
R_T = 90 kΩ		C_{OUT1} = 47 µF, elyt
R_S = 18 kΩ		C_{OUT2} = 470 nF, cer
R_{FB} = 30 kΩ		C_{SOFT} = 2.2 nF 50V, cer
R_A = 20 kΩ		C_{FB} = 10 nF 50V, cer
R_L = 3 kΩ		C_{BB} = 100 nF 50V, cer
R_{SNS} = 0.39 Ω		C_{EE} = 100nF 50V, cer
L_1 = 68 µH, 1A		
L_2 = 10 µH, 1A		
D_1 = 1A, 90V schottky		
Optional input filter:		C_{IN} = 330n, cer
		L_{IN} = 10µH, 1A

Example of choosing external components

Component	**Manufacture**	**Part number**	**Value**
L_1 , L_{IN}	KOA	LPC4045TE 100K	10µH 1.02A
L_2	KOA	LPC9040TE 680K	68µH 0.91A
D_1	Telefunken	BYS11-90	90V 1.5A Schottky
D_1	Motorola	MBRS1100T3	100V 1A Schottky
R_{SNS}	KOA	SR73K2ATDJ0,39OHM	0.39Ω
R_{SNS}	Draloric	D12200 0.39 5%P5	0.39Ω 5%

Thermal management

Detailed layout recommendations will be available with the test board.

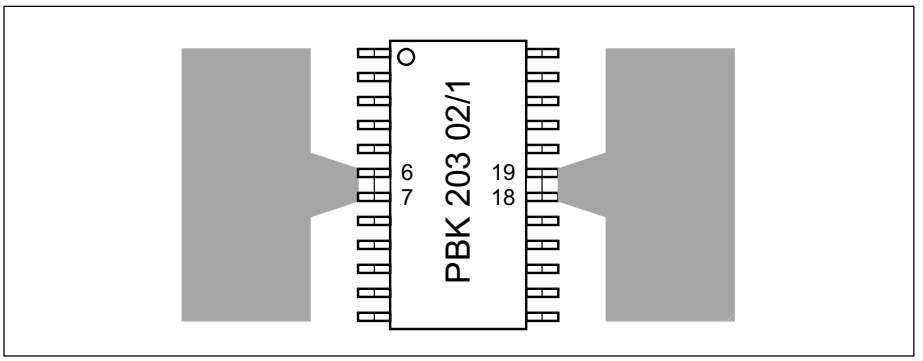


Figure 5 Recommended PCB layout for cooling.

Specifications subject to change without notice.

1522-PBK 203 02/1 Uen Rev. C

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